

FORM PTO-1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		ATTY. DOCKET NO. 1778.0200000	APPLICATION NO. 09/836,541
		FIRST NAMED INVENTOR Ryan C. Kinter	
		FILING DATE April 18, 2001	ART UNIT 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
~	AA1	3,631,405	12/1971	Hoff et al.			
~	AB1	3,794,980	02/1974	Cogar et al.			
~	AC1	3,811,114	05/1974	Lemay et al.			
~	AD1	3,840,861	10/1974	Amdahl et al.			
~	AE1	3,983,541	09/1976	Faber et al.			
~	AF1	4,110,822	08/1978	Porter et al.			
~	AG1	4,149,244	04/1979	Anderson et al.			
~	AH1	4,229,790	10/1980	Gilliland et al.			
~	AI1	4,295,193	10/1981	Pomerene, James H.			
~	AJ1	4,432,056	02/1984	Almura, Harutsugu			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
~	AK1	EP 0 073 424 A2	03/1983	Europe			N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

~	AO1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).
~	AP1	Preliminary Amendment, filed February 1, 2002, in U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (15 pages).
~	AQ1	Case, Brian, "ARM Architecture Offers High Code Density: Non-Traditional RISC Encodes Many Options in Each Instruction," <i>Microprocessor Report</i> , Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 SEP 20 2005 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT U.S. PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 1778.0200000	APPLICATION NO. 09/836,541
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		FILING DATE April 18, 2001	ART UNIT 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
h	AA2	4,467,409	08/1984	Potash et al.			
h	AB2	4,507,728	03/1985	Sakamoto et al.			
h	AC2	4,685,080	08/1987	Rhodes, Jr. et al.			
h	AD2	4,724,517	02/1988	May, Michael D.			
h	AE2	4,777,594	10/1988	Jones et al.			
h	AF2	4,782,441	11/1988	Inagami et al.			
h	AG2	4,876,639	10/1989	Mensch Jr., William D.			
h	AH2	5,132,898	07/1992	Sakamura et al.			
h	AI2	5,241,636	08/1993	Kohn, Leslie D.			
h	AJ2	5,355,460	10/1994	Eickemeyer et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
T	AK2	EP 0 239 081 B1	09/1995	Europe			N/A
h	AL2	EP 0 324 308 B1	03/1996	Europe			N/A
h	AM2	EP 0 368 332 B1	09/1997	Europe			N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

h	AN2	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor Forum, 13 slides (7 pages) (October 22-23, 1996).
h	AO2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).
h	AP2	Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," <i>Logic Programming: Proceedings of the Fifth International Conference and Symposium</i> (August 15-19, 1988), MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).
h	AQ2	NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright NEC Electronics Corporation 2000) (76 pages).
h	AR2	NEC User's Manual, VR4100 Series™, 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 (Chapter 3) (Copyright NEC Corporation 2002).

EXAMINER	<i>[Signature]</i>	DATE CONSIDERED
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USPTO

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
<i>CR</i>	AA3	5,506,974	04/1996	Church et al.			
<i>CR</i>	AB3	5,574,873	11/1996	Davidian, Gary G.			
<i>CR</i>	AC3	5,732,234	03/1998	Vassiliadis et al.			
<i>CR</i>	AD3	5,740,461	04/1998	Jagger, David Vivian			
<i>CR</i>	AE3	6,021,265	02/2000	Nevill, Edward Colles			
<i>CR</i>	AF3	6,266,765 B1	07/2001	Horst, Robert W.			07/07/2000
<i>CR</i>	AG3	6,272,620 B1	08/2001	Kawasaki et al.			04/04/2000
<i>CR</i>	AH3	2001/0021970 A1	09/2001	Hotta et al.			05/14/2001
<i>CR</i>	AI3	2004/0054872 A1	03/2004	Nguyen et al.			09/12/2003
<i>CR</i>	AJ3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
<i>CR</i>	AK3	EP 0 449 661 B1	11/1995	Europe			N/A
<i>CR</i>	AL3	GB 2 016 755 A	09/1979	United Kingdom			N/A
	AM3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

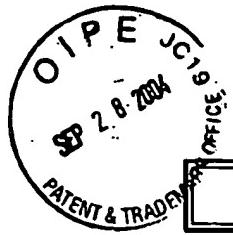
<i>CR</i>	AN3	NEC User's Manual, VR4121™, 64/32-Bit Microprocessor, uPD30121, pp. 1-19 and 103-131 (Chapter 4) (Copyright NEC Corporation 1998).
<i>CR</i>	AO3	Ross, Roger, "There's no risk in the future for RISC," Computer Design, Vol. 28, No. 22, pp. 73-75 (November 13, 1989).
	AP3	
	AQ3	
	AR3	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE	
AA1							
AB1							
AC1							
AD1							
AE1						RECEIVED	
AF1						SEP 20 2001	
AG1						TECHNOLOGY REVIEWED	
AH1							
AI1							
AJ1							
AK1							
FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
AL1	0 109 567 A2	05/1984	EPO			N/A	
AM1	0 170 398 A2	02/1986	EPO			N/A	
AN1	WO 95/30187 A1	11/1995	WO			N/A	
AO1						Yes No	
AP1						Yes No	
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
AR	1	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads," ACM SIGARCH Computer Architecture News, Volume 20, Number 2, pgs. 136-145, Association for Computing Machinery (May 1992).					
AS	1						
AT	1						
EXAMINER				DATE CONSIDERED			
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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

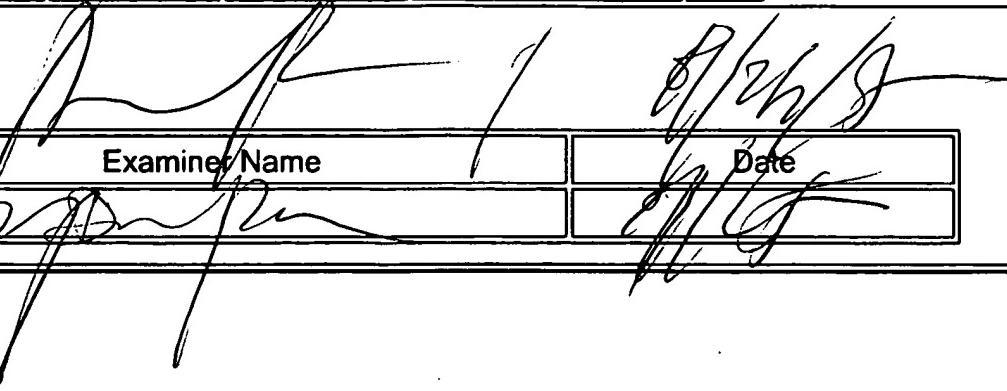
Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Mapping System and Method for Instruction Set Processing				
Application Number:	09/836541		 RECEIVED		
Confirmation Number:	6813		OCT 04 2004		
First Named Applicant:	Ryan KINTER				
Attorney Docket Number:	1778.0200000				
Art Unit:	2183		Technology Center 2100		
Examiner:	Daniel H. Pan				
Search string:	(4388682 or 4484268 or 5031096 or 5115500 or 5371864 or 5392408 or 5394558 or 5396634 or 5404472 or 5475824 or 5475853 or 5542060 or 5568646 or 5574941 or 5581718 or 5619667 or 5664136 or 5796973 or 5954830 or 6651160),pn.				
US Patent Documents					
Note: Applicant is not required to submit a paper copy of cited US Patent Documents					
init	Cite.No.	Patent No.	Date	Patentee	Kind
1	1	4388682	1983-06-14	Eldridge	Class
2	2	4484268	1984-11-20	Thoma et al.	Subclass
3	3	5031096	1991-07-09	Jen et al.	
4	4	5115500	1992-05-19	Larsen	
5	5	5371864	1994-12-06	Chuang	
6	6	5392408	1995-02-21	Fitch	
7	7	5394558	1995-02-28	Arakawa et al.	
8	8	5396634	1995-03-07	Zaidi et al.	
9	9	5404472	1995-04-04	Kurosawa et al.	
10	10	5475824	1995-12-12	Grochowski et al.	
11	11	5475853	1995-12-12	Blaner et al.	
12	12	5542060	1996-07-30	Yoshida	
13	13	5568646	1996-10-22	Jaggar	
14	14	5574941	1996-11-12	Horst	

15	5581718	1996-12-03	Grochowski
16	5619667	1997-04-08	Henry et al.
17	5664136	1997-09-02	Witt et al.
18	5796973	1998-08-18	Witt et al.
19	5954830	1999-09-21	Ternullo, Jr.
20	6651160	2003-11-18	Hays
			B1

Signature



Examiner Name	Date
